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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,593	11/19/2003	David Walter Flynn	550-488	6450

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EXAMINER	
PRETLOW, DEMETRIUS R	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,593	FLYNN, DAVID WALTER	
	Examiner	Art Unit	
	Demetrius R. Pretlow	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-25,27-41 and 44-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-25,27-41 and 44-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *9/22/06* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Non Final Rejection mailed June 21, 2006 is withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 45 recites the limitation "said clock generator" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claims 47recites the limitation "said clock generator" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-5, 7-25,27-41 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 2-41 of copending Application No. 11/430903. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

1. Apparatus for processing data, said apparatus comprising: a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level, wherein said mapping circuit performs at least one many to one mapping between performance level request signal values and corresponding control signal values.	6. Apparatus for processing data, said apparatus comprising: a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level, wherein said mapping circuit performs a many to one mapping between performance level request signal values and corresponding control signal values.
2. Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to	2. Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to

drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected. 3. Apparatus as claimed in claim 1, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected. 4. Apparatus as claimed in claim 1, wherein said control signal is a thermometer coded value. 5. Apparatus as claimed in claim 4, having a plurality of processors and mapping circuits operable to generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or more further circuits. 7. Apparatus as claimed in claim 1, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level request signal values mapped to	drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected. 3. Apparatus as claimed in claim 1, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected. 4. Apparatus as claimed in claim 1, wherein said control signal is a thermometer coded value. 5. Apparatus as claimed in claim 4, having a plurality of processors and mapping circuits operable to generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or more further circuits. 7. Apparatus as claimed in claim 6, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level request signal values mapped to

said control signal value.	said control signal value.
8. Apparatus as claimed in claim 1, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value.	8. Apparatus as claimed in claim 1, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value.
9. Apparatus as claimed in claim 1, wherein at least one of said one or more further circuits operates in a different clock domain to said processor.	9. Apparatus as claimed in claim 1, wherein at least one of said one or more further circuits operates in a different clock domain to said processor.
10. Apparatus as claimed in claim 1, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values.	10. Apparatus as claimed in claim 1, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values.
11. Apparatus as claimed in claim 10, wherein said configuration values specify voltage levels corresponding to different control signal values.	11. Apparatus as claimed in claim 3, wherein said configuration values specify voltage levels corresponding to different control signal values.
12. Apparatus as claimed in claim 1, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at at least one intermediate data processing	12. Apparatus as claimed in claim 1, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at at least one intermediate data processing

performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.	performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.
13. Apparatus as claimed in claim 2, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.	13. Apparatus as claimed in claim 2, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.
14. Apparatus as claimed in claim 12, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.	14. Apparatus as claimed in claim 12, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.
15. Apparatus as claimed in claim 1, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.	15. Apparatus as claimed in claim 1, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.
16. Apparatus as claimed in claim 3, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage	16. Apparatus as claimed in claim 3, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage

controller.	controller.
17. Apparatus as claimed in claim 2, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.	17. Apparatus as claimed in claim 2, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.
18. Apparatus as claimed in claim 2, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.	18. Apparatus as claimed in claim 2, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.
19. Apparatus as claimed in claim 18, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.	19. Apparatus as claimed in claim 18, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.
20. Apparatus as claimed in claim 16, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.	20. Apparatus as claimed in claim 16, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.
21. A method of processing	26. A method of processing

data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level. 22. A method as claimed in claim 21, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.	data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level, wherein said mapping is a many to one mapping between performance level request signal values and corresponding control signal values. 22. A method as claimed in claim 21, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing

23. A method as claimed in claim 21, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected. 24. A method as claimed in claim 21, wherein said control signal is a thermometer coded value. 25. A method as claimed in claim 24, wherein a plurality of processors and mapping circuits generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or more further circuits. 27. A method as claimed in claim 21, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level request signal values mapped to said control signal value. 28. A method as claimed in claim 21, wherein performance	operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected. 23. A method as claimed in claim 21, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected. 24. A method as claimed in claim 21, wherein said control signal is a thermometer coded value. 25. A method as claimed in claim 24, wherein a plurality of processors and mapping circuits generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or more further circuits. 27. A method as claimed in claim 26, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level

level supported as controlled by control signal value increases monotonically with performance level request signal value. 29. A method as claimed in claim 21, wherein at least one of said one or more further circuits operates in a different clock domain to said processor. 30. A method as claimed in claim 21, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values. 31. A method as claimed in claim 30, wherein said configuration values specify voltage levels corresponding to different control signal values. 32. A method as claimed in claim 21, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one	request signal values mapped to said control signal value. 28. A method as claimed in claim 21, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value. 29. A method as claimed in claim 21, wherein at least one of said one or more further circuits operates in a different clock domain to said processor. 30. A method as claimed in claim 21, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values. 31. A method as claimed in claim 23, wherein said configuration values specify voltage levels corresponding to different control signal values. 32. A method as claimed in claim 21, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data

intermediate data processing performance level during said change. 33. A method as claimed in claim 22, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency. 34. A method as claimed in claim 32, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal. 35. A method as claimed in claim 21, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit. 36. A method as claimed in claim 23, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller. 37. A method as claimed in	processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change. 33. A method as claimed in claim 22, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency. 34. A method as claimed in claim 32, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal. 35. A method as claimed in claim 21, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit. 36. A method as claimed in claim 23, wherein said current operation signal is indicative of a maximum power supply

claim 22, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator. 38. A method as claimed in claim 22, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies. 39. A method as claimed in claim 38, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies. 40. A method as claimed in claim 36, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency. 41. A computer program product containing program instructions for controlling a processor to	voltage of that can currently be supported by said voltage controller. 37. A method as claimed in claim 22, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator. 38. A method as claimed in claim 22, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies. 39. A method as claimed in claim 38, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies. 40. A method as claimed in claim 36, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock

operate in accordance with the method as claimed in claim 22.	signal frequency. 41. A computer program product containing program instructions for controlling a processor to operate in accordance with the method as claimed in claim 22.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 44-47 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,2,18,21,22,28 and 38 of copending Application No. 11/430903. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 44-47 are anticipated by claim 1,2,18,21,22,28 and 38.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10/715593	11/430903
44. Apparatus for processing data, said apparatus comprising:a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling	1. Apparatus for processing data, said apparatus comprising: a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet

generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level, wherein performance level supported as controlled by control signal value changes monotonically with performance level request signal value.	said desired data processing performance level, 8. Apparatus as claimed in claim 1, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value.
45. Apparatus for processing data, said apparatus comprising: a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or	1. Apparatus for processing data, said apparatus comprising: a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance, 2. Apparatus as claimed in claim 2, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a

more further circuits are controlled to meet said desired data processing performance level, wherein said clock generator is operable to generate a clock signal with one or more available clock signal frequencies and one or more selectively available clock signal frequencies.	selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.
46. A method of processing data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired	21 A method of processing data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level. 28. A method as claimed in claim 21, wherein performance level supported as controlled

data processing performance level, wherein performance level supported as controlled by control signal value changes monotonically with performance level request signal value. 47. A method of processing data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level, wherein said clock generator is operable to generate a clock	by control signal value increases monotonically with performance level request signal value. 21. A method of processing data, said method comprising the steps of: performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level. 22. A method as claimed in claim 21, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing

signal with one or more available clock signal frequencies and one or more selectively available clock signal frequencies.	operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Demetrius R. Pretlow Demetrius Pretlow 12/15/06

Patent Examiner

John Barlow
Supervisory Patent Examiner
Technology Center 2800